**IN THE CLAIMS**:

Claim 83 is canceled herein. Claims 1, 72, 103 and 105 have been amended herein. All of the pending claims 1-27, 72-82 and 84-106 are presented below. This listing of claims will replace all prior versions and listings of claims in the application. Please enter these claims as amended.

1. (Amended four times) A method for making a metallization structure for a semiconductor device, comprising:

forming a substantially planar first dielectric layer on a substrate;

forming at least one metal containing barrier layer over the first dielectric layer;

E1 forming a single conducting layer ~~over~~on the at least one metal containing barrier layer;

forming a second dielectric layer in contact with the single conducting layer;

removing aligned portions of the second dielectric layer, single conducting layer, and at least one metal containing barrier layer to form a multilayer structure; and

forming metal containing spacers on sidewalls of the multilayer structure, said metal containing spacers ~~being substantially the same height as said multilayer structure~~beginning at a lower surface of said at least one metal containing barrier layer and extending substantially to an upper surface of said second dielectric layer.

2. (Previously amended) The method of claim 1, wherein said forming the first dielectric layer comprises forming a silicon oxide or BPSG layer.

3. (Previously amended three times) The method of claim 2, wherein said forming the at least one metal containing barrier layer comprises forming the at least one metal containing barrier layer of Ti, Ta, W, Co or Mo or an alloy or a compound of any thereof, including TaN or TiN.

4. (Previously amended four times) The method of claim 3, further comprising forming a second metal containing barrier layer between a first metal containing barrier layer of said at least one metal containing barrier layer and the substrate, said second metal containing barrier layer comprising TiN, TiW, WN, or TaN.

5. (Previously amended three times) The method of claim 1, wherein said forming the at least one metal containing barrier layer comprises forming the at least one metal containing barrier layer of titanium or titanium nitride.

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6. (Previously amended twice) The method of claim 1, wherein the at least one metal containing barrier layer is a single metal containing barrier layer and further comprising forming the single metal containing barrier layer of titanium or titanium nitride.

7. (Previously amended twice) The method of claim 1, wherein said forming the single conducting layer comprises forming the single conducting layer from at least one of aluminum and copper.

8. (Previously amended twice) The method of claim 7, wherein said forming the single conducting layer comprises forming the single conducting layer of an aluminum-copper alloy.

9. (Previously amended twice) The method of claim 1, wherein said forming the metal containing spacers comprises forming at least one layer of Ti, Ta, W, Co or Mo, or alloys thereof or compounds thereof, including TaN and TiN.

10. (Previously amended twice) The method of claim 9, wherein said forming the metal containing spacers comprises forming the metal containing spacers of titanium or titanium nitride.

11. (Previously amended three times) The method of claim 1, wherein said forming a second dielectric layer comprises forming the second dielectric layer on the single conducting layer to have sidewalls aligned with sidewalls of the single conducting layer, and forming the metal containing spacers to extend along the sidewalls of the second dielectric layer.

12. (Previously amended) The method of claim 11, further comprising forming the second dielectric layer of a low dielectric constant material.

13. (Previously amended) The method of claim 12, further comprising forming the second dielectric layer of a fluorine-doped silicon oxide.

14. (Previously amended twice) The method of claim 1, further comprising forming the at least one metal containing barrier layer and the metal containing spacers of a same metal.

15. (Previously amended three times) The method of claim 1, wherein said forming the at least one metal containing barrier layer comprises forming the at least one metal containing barrier layer by vapor deposition.

16. (Previously amended four times) The method of claim 1, wherein said forming the at least one metal containing barrier layer comprises forming the at least one metal containing barrier layer by CVD, PVD or PECVD.

17. (Previously amended twice) The method of claim 1, wherein said forming the single conducting layer comprises forming the single conducting layer by vapor deposition.

18. (Previously amended) The method of claim 17, further comprising forming the single conducting layer by CVD, PVD or PECVD.

19. (Previously amended twice) The method of claim 1, wherein said forming the metal containing spacers comprises forming the metal containing spacers by vapor deposition and directional etching.

20. (Original) The method of claim 19, further comprising effecting the vapor deposition as CVD, PVD or PECVD.

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21. (Previously amended three times) The method of claim 1, wherein removing aligned portions of the second dielectric layer, single conducting layer, and at least one metal containing barrier layer to form the multilayer structure is effected by patterning and etching the second dielectric layer, the single conducting layer, and the at least one metal containing barrier layer.

22. (Previously amended three times) The method of claim 1, wherein said forming the metal containing spacers comprises forming a metal containing spacer layer over the multilayer structure and first dielectric layer and removing portions thereof overlying the first and second dielectric layers.

23. (Previously amended three times) The method of claim 22, wherein said forming the metal containing spacers comprises forming the metal containing spacer layer over the multilayer structure and first dielectric layer by a conformal deposition process.

24. (Previously amended twice) The method of claim 23, wherein portions of the metal containing spacer layer over the multilayer structure and first dielectric layer are removed by etching.

25. (Previously amended twice) The method of claim 1, further comprising removing any remaining portion of the second dielectric layer and upper portions of the metal containing spacers laterally adjacent thereto to expose said single conducting layer.

26. (Previously amended twice) The method of claim 25, further comprising removing any remaining portion of the second dielectric layer and upper portions of the metal containing spacers by etching.

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27-71 (Canceled)

72. (Amended three times) A method for constructing a metallization structure for a semiconductor device, comprising:

providing a substrate having a first dielectric layer underlying at least one metal containing barrier layer;

creating a single conducting layer over the at least one metal containing barrier layer, said single conducting layer comprising at least copper or aluminum and comprising an upper surface, said upper surface of said single conducting layer out of contact with any metal;

removing aligned portions of the single conducting layer and at least one metal containing barrier layer to form a multilayer structure; and

flanking at least one surface of the multilayer structure with a metal containing spacer, said metal containing spacer extending to substantially the same height as said single conducting layer.

73. (Previously amended twice) The method of claim 72, further comprising forming a second dielectric layer in contact with said single conducting layer.

74. (Previously added) The method of claim 73, wherein said removing further comprises removing aligned portions of said second dielectric layer to form said multilayered structure.

75. (Previously amended) The method of claim 73, wherein said flanking at least one surface of the multilayer structure with a metal containing spacer comprises forming a metal containing spacer layer on said second dielectric layer.

76. (Previously amended) The method of claim 75, further comprising removing any remaining portion of the second dielectric layer and upper portions of the metal containing spacer layer laterally adjacent thereto.

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77. (Previously added) The method of claim 76, wherein said removing any remaining portion is effected by etching.

78. (Previously amended) The method of claim 72, wherein said providing a substrate having a first dielectric layer comprises forming said first dielectric layer of a silicon oxide or BPSG layer.

79. (Previously amended twice) The method of claim 72, wherein said providing a substrate having a first dielectric layer underlying at least one metal containing barrier layer comprises forming the at least one metal containing barrier layer of Ti, Ta, W, Co or Mo or an alloy or a compound of any thereof, including TaN or TiN.

80. (Previously amended twice) The method of claim 79, wherein said forming the at least one metal containing barrier layer comprises forming the at least one metal containing barrier layer of titanium or titanium nitride.

81. (Previously amended twice) The method of claim 72, further comprising forming a second metal containing barrier layer between a first metal containing barrier layer of the at least one metal containing barrier layer and the substrate, said second metal containing barrier layer comprising TiN, TiW, WN, or TaN.

82. (Previously amended twice) The method of claim 72, wherein the at least one metal containing barrier layer is a single metal containing barrier layer and further comprising forming the single metal containing barrier layer of titanium or titanium nitride.

83. (Canceled herein)

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84. (Previously amended) The method of claim 72, wherein said creating a single conducting layer comprises creating the single conducting layer of an aluminum-copper alloy.

85. (Previously amended) The method of claim 72, wherein said flanking comprises forming the metal containing spacer of at least one layer of Ti, Ta, W, Co or Mo, or alloys thereof or compounds thereof, including TaN and TiN.

86. (Previously amended) The method of claim 85, wherein said forming the metal containing spacer comprises forming the metal containing spacers of titanium or titanium nitride.

87. (Previously amended twice) The method of claim 72, wherein said flanking at least one surface comprises forming said metal containing spacer on sidewalls of said multilayer structure.

88. (Previously amended) The method of claim 72, wherein said flanking at least one surface comprises forming said metal containing spacer on a top surface of said multilayer structure.

89. (Previously amended twice) The method of claim 72, further comprising forming a second dielectric layer on the single conducting layer to have sidewalls aligned with the conductive layer sidewalls, and forming the metal containing spacer to extend along the sidewalls of the second dielectric layer.

90. (Previously added) The method of claim 89, wherein said forming the second dielectric layer comprises forming the second dielectric layer of a low dielectric constant material.

91. (Previously added) The method of claim 90, wherein said forming the second dielectric layer comprises forming the second dielectric layer of a fluorine-doped silicon oxide.

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92. (Previously amended twice) The method of claim 72, further comprising forming the at least one metal containing barrier layer and the metal containing spacer of a same metal.

93. (Previously amended twice) The method of claim 72, wherein said providing a substrate having a first dielectric layer underlying at least one metal containing barrier layer comprises forming the at least one metal containing barrier layer by vapor deposition.

94. (Previously amended twice) The method of claim 93, wherein said forming the at least one metal containing barrier layer by vapor deposition comprises forming the at least one metal containing barrier layer by CVD, PVD or PECVD.

95. (Previously amended) The method of claim 72, wherein said creating a single conducting layer comprises forming the conducting layer by vapor deposition.

96. (Previously amended) The method of claim 95, wherein said forming the single conducting layer by vapor deposition comprises forming the single conducting layer by CVD, PVD or PECVD.

97. (Previously amended) The method of claim 72, wherein said flanking comprises forming the metal containing spacer by vapor deposition and directional etching.

98. (Previously added) The method of claim 97, further comprising effecting the vapor deposition as CVD, PVD or PECVD.

99. (Previously amended twice) The method of claim 72, wherein removing aligned portions of the single conducting layer and at least one metal containing barrier layer to form a multilayer structure is effected by patterning and etching the single conducting layer and the at least one metal containing barrier layer.

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100. (Previously amended) The method of claim 72, wherein said flanking comprises forming the metal containing spacer by forming a metal containing spacer layer over the multilayer structure and first dielectric layer and removing portions thereof overlying the first dielectric layer and a top portion of said multilayer structure.

101. (Previously amended twice) The method of claim 100, wherein said forming the metal containing spacer layer over the multilayer structure and first dielectric layer comprises forming the metal containing layer by a conformal deposition process.

102. (Previously amended) The method of claim 101, wherein said removing portions of the metal containing spacer layer is effected by etching.

103. (Amended twice) A method for making a metallization structure for a semiconductor device, comprising:

forming a substantially planar first dielectric layer on a substrate;

forming at least one metal containing barrier layer over the first dielectric layer;

forming a single conducting layer over the at least one metal containing barrier layer;

forming a second dielectric layer in contact with the single conducting layer;

removing aligned portions of the second dielectric layer, the single conducting layer, and the at least one metal containing barrier layer to form a multilayer structure;

forming metal containing spacers on sidewalls of the multilayer structure; and

removing any remaining portion of the second dielectric layer and upper portions of the metal containing spacers laterally adjacent thereto.

104. (Previously added) The method of claim 103, wherein said removing any remaining portion is effected by etching.

105. (Amended twice) A method for constructing a metallization structure for a semiconductor device, comprising:

providing a substrate having a first dielectric layer underlying at least one metal containing barrier layer;

creating a conducting layer ~~over~~on the at least one metal containing barrier layer;

forming a second dielectric layer on said conducting layer;

removing aligned portions of the second dielectric layer, the conducting layer and the at least one metal containing barrier layer to form a multilayer structure;

flanking at least one surface of the multilayer structure with a metal containing spacer such that said metal containing spacer is substantially the same height as said ~~conducting~~second dielectric layer; and

removing any remaining portion of the second dielectric layer and upper portions of the metal containing spacer layer laterally adjacent thereto.

106. (Previously added) The method of claim 105, wherein said removing any remaining portion is effected by etching.